User Manual

GHD3125R

Three-phase 36V Gate Driver

Version: V1.0

Contents

1 Product Overview

1.1 Introduction

GHD3125R is a three-phase 36V gate drive integrated circuit used to drive P/NMOS power transistors, and is suitable for DC brushless motor applications such as low-voltage fans and water pumps. This chip integrates 5V LDO, has a current-carrying capacity of 60mA, and can provide power for internal logic circuits and external MCU. Multiple protection functions are built in GHD3125R, including undervoltage protection, input straight-through protection, and startup protection. It has a dead time of 400ns to effectively ensure normal operation of the system. At the same time, it provides an output driving voltage of 11V, has excellent sink current capability, and can effectively drive the external P/NMOS power transistors.

1.2 Main characteristics

- Three-phase gate driver for P/NMOS power transistors
- Recommended range of supply voltage: 5.5V~30V
- Built-in 5V/60mA LDO
- HO output current+260mA/-80mA@V_{sup}=24V
- LO output current+50mA/-240mA@V_{sup}=24V
- Low standby power consumption
- 3.3V/5V input logic compatibility
- LDO overload start protection
- Built-in power undervoltage protection UVLO
- Built-in straight-through prevention function
- Built-in 400ns dead time
- Matching of high and low-side channels

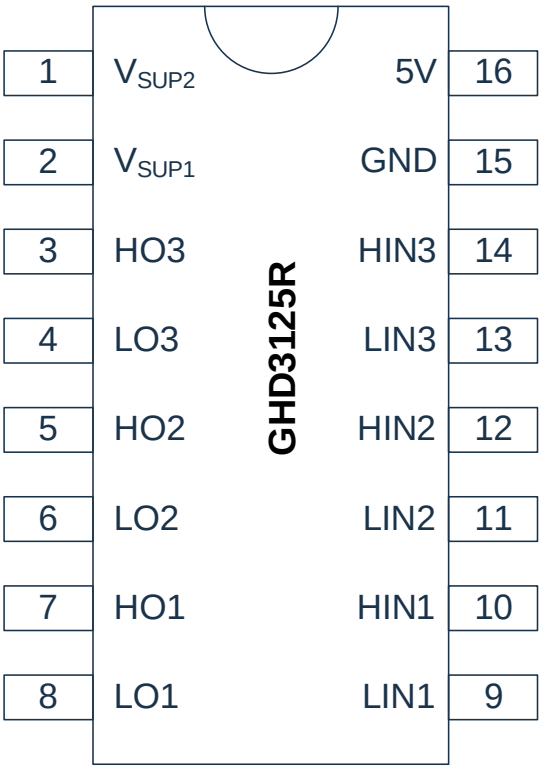
1.3 Application scope

Widely used in DC brushless motor systems such as floor fans and circulating pumps.

2 Pin Information

2.1 Pin distribution

Figure 1 Distribution Diagram of GHD3125R Pins



2.2 Pin functional description

Table 1 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in the bracket below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type	P	Power pin or ground
	I	Only input pin
	O	Only output pin

Table 2 Description of Sorting by Pin Number of GHD3125R

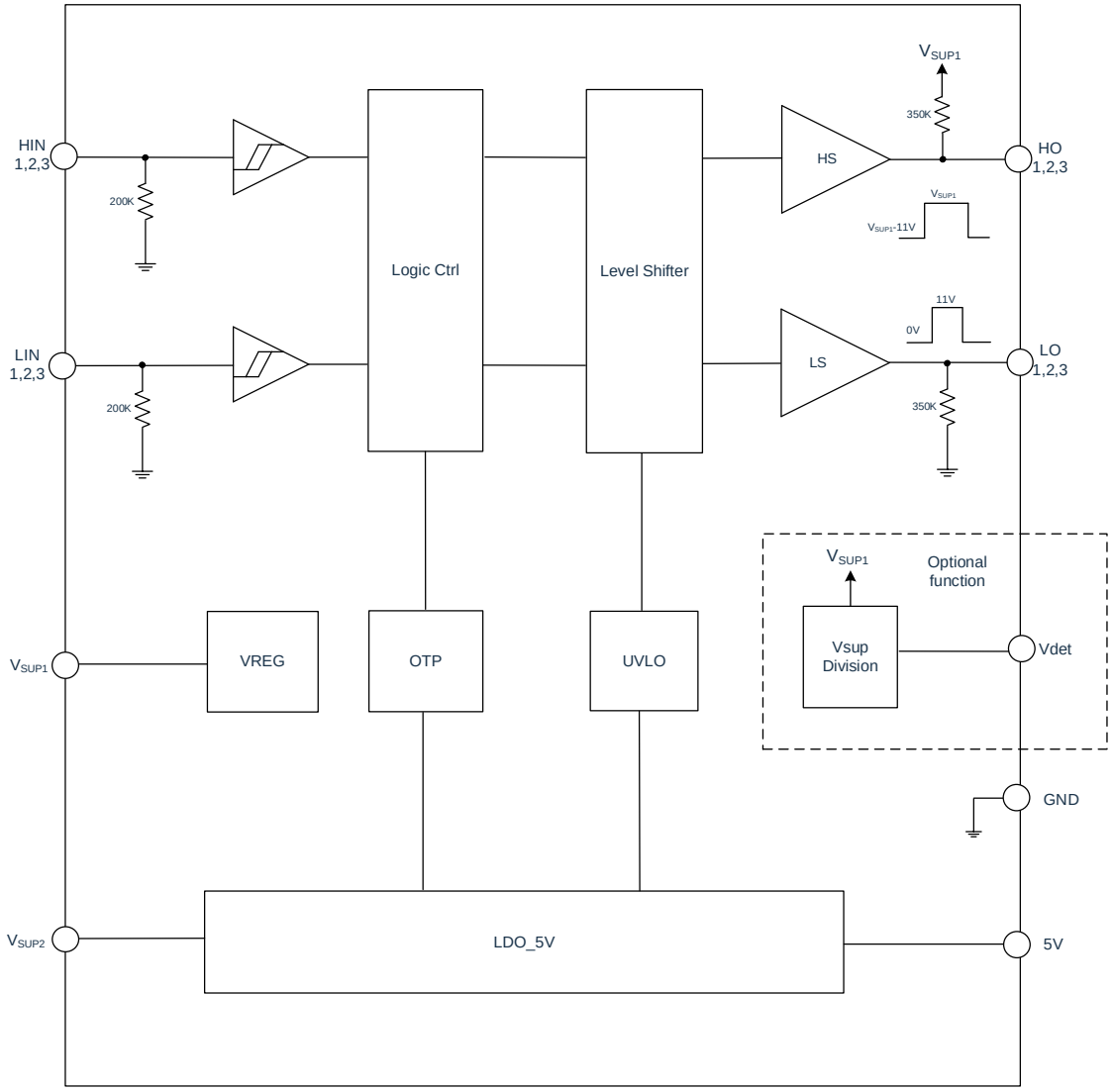
Name	Type	Functional description	Pin No.
V_{SUP2}	P	LDO power supply terminal	1
V_{SUP1}	P	Drive power supply terminal	2
HO3	O	Phase 3 high-side output	3

Name	Type	Functional description	Pin No.
LO3	O	Phase 3 low-side output	4
HO2	O	Phase 2 high-side output	5
LO2	O	Phase 2 low-side output	6
HO1	O	Phase 1 high-side output	7
LO1	O	Phase 1 low-side output	8
LIN1	I	Phase 1 low-side input	9
HIN1	I	Phase 1 high-side input	10
LIN2	I	Phase 2 low-side input	11
HIN2	I	Phase 2 high-side input	12
LIN3	I	Phase 3 low-side input	13
HIN3	I	Phase 3 high-side input	14
GND	P	Grounding end of the chip	15
5V	P	5V output end (external stabilizing capacitor, supplying power to MCU)	16

3 Block Diagram Logic

3.1 Internal block diagram

Figure 2 GHD3125R Internal Block Diagram



3.2 Logic truth value

Table 3 Logic Truth Value

LIN	HIN	LO	HO
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	OFF	OFF
Suspension	Suspension	OFF	OFF

Note:

(1) 1: Logic high level, 0: Logic low level.

(2) ON: V_{HO}=V_{SUP1}-11V, V_{LO}=11V OFF: V_{HO}=V_{SUP1}, V_{LO}=0V.

(3) It is recommended to maintain a strong input state at the input port to avoid unstable states such as high resistance and suspension.

4 Electrical Characteristics

4.1 Recommended safe operating range

T_A=25℃; unless otherwise specified, all pins take GND as the reference points.

Table 4 General Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{SUP1}	5V supply voltage	5.5	24	30	V
V_{SUP2}	Driving supply voltage	5.5	24	30	V
V_{IN}	Input voltage (HIN/LIN)	0	-	5	V
T_A	Ambient temperature (Note 1)	-40	-	85	℃

Note:

(1) T_A represents the ambient temperature at which the circuit operates.

(2) Operation beyond the recommended conditions for a long time may affect its reliability.

4.2 Absolute maximum rated value

T_A=25℃; unless otherwise specified, all pins take GND as the reference points. When the specified range of the absolute maximum rated value is exceeded, permanent damage may be caused to the chip.

Table 5 Power Consumption

Symbol	Description	MIN	MAX	Unit
P_D	Maximum power consumption	-	1.4	W

Note:

(1) At any time, the power consumption cannot exceed P_D. The calculation formula for the maximum power consumption at different ambient temperatures is: P_D=(150℃-T_A)/ θ_{JA}。

(2) 150℃ is the maximum operating junction temperature of the circuit, T_A is the operating ambient temperature of the circuit, and θ_{JA} is the thermal resistance of the package.

Table 6 Temperature Characteristics

Symbol	Description	MIN	MAX	Unit
T_s	Storage temperature	-55	150	℃
θ_{JA}	Junction-to-ambient thermal resistance	-	89	℃/W
T_J	Junction temperature	-	150	℃
T_L	Pin welding temperature (duration 10s)	-	260	℃

Table 7 Maximum Rated Voltage Characteristics

Symbol	Description	MIN	MAX	Unit
V_{SUP1}	Driving supply voltage	-0.3	40	V
V_{SUP2}	5V supply voltage	-0.3	40	

Symbol	Description	MIN	MAX	Unit
V_{LDO}	LDO output voltage	-0.3	5.5	
V_{HO}	High-side output voltage	V_{SUP1}-14	V_{SUP1}+0.3	
V_{LO}	Low-side output voltage	-0.3	14	
V_{IN}	Logic input voltage	-0.3	5.5	

Table 8 Maximum Rated Current Characteristics

Symbol	Description	MIN	MAX	Unit
I_{load}	LDO output current	0	100	mA

Table 9 ESD Characteristics

Symbol	Description	MIN	MAX	Unit
$V_{ESD\ (HBM)}$	Electrostatic discharge voltage (human body model)	-	2000	V

Note: For human body model, the 100pF capacitor is discharged through a 1.5kΩ resistor.

4.3 Electrical characteristic parameters

T_A=25℃, V_{SUP1}=V_{SUP2}=V_{SUP}=24V, the ground capacitance of GND=0 V_{SUP} and the ground resistance of 5V are both 1 μF, and unless otherwise specified, all pins take GND as the reference point.

Table 10 Supply Voltage Parameters

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{SUPHY+}	V_{SUP} undervoltage high-level potential	3.8	4.0	4.4	V
V_{SUPHY-}	V_{SUP} undervoltage low-level potential	3.6	3.8	4.2	V
V_{SUPHY}	V_{SUP} undervoltage hysteresis level	0.1	0.2	0.4	V

Table 11 Supply Current Parameters

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
I_{SUPQ}	V_{SUP} quiescent current	V_{HIN}=V_{LIN}=0	500	650	1000	μA
I_{SUPD}	V_{SUP} dynamic current	f_{VIN}=20kHz	0.8	2.0	3.5	mA

Table 12 Time Parameters

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
T_{ON}	Output rising edge transmission time	No Load	170	230	400	ns
T_{OFF}	Output falling edge transmission time	No Load	110	150	300	ns
T_{rise_H}	Output rise time of HO	C_L=1nF	30	60	100	ns
T_{fall_H}	Output fall time of HO	C_L=1nF	200	270	350	ns
T_{rise_L}	Output rise time of LO	C_L=1nF	250	340	420	ns
T_{fall_L}	Output fall time of LO	C_L=1nF	55	85	110	ns
DT	Dead time	No Load	250	400	600	ns
MT	High and low-side matching time	ΔT_{ON} & $\Delta TOFF$	-	-	100	ns

Table 13 Input-end Parameters

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
I_{IN+}	Input high-level current	V_{HIN} or V_{LIN}=5V	15	25	35	μA
I_{IN-}	Input low-level current	V_{HIN} or V_{LIN}=0	-1	0	1	μA
V_{IN+}	Input high-level potential	-	1.7	2.1	2.6	V
V_{IN-}	Input low-level potential	-	0.7	1.0	1.3	V
V_{INHY}	Input hysteresis level	-	0.7	1.1	1.5	V

Table 14 Output-end Parameters

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
I_{HO+}	HO output current	V_{HIN}=0, V_{HO}=V_{SUP}, PWD≤10μs	200	260	350	mA
I_{HO-}	HO sink current	V_{HIN}=5V, V_{HO}=V_{SUP}-11V, PWD≤10μs	65	80	95	mA
I_{LO+}	LO output current	V_{LIN}=5V, V_{LO}=0, PWD≤10μs	35	50	65	mA
I_{LO-}	LO sink current	V_{LIN}=0, V_{LO}=11V, PWD≤10μs	200	240	280	mA
V_{HO}	HO output voltage	V_{LIN}=0V, V_{HIN}=5V	V_{SUP}-13	V_{SUP}-11	V_{SUP}-9	V
V_{LO}	LO output voltage	V_{LIN}=5V, V_{HN}=0V	9	11	13	V

Table 15 LDO Parameters

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
V_{5V}	Output voltage range	V_{SUP}=5.5V~30V	4.8	5.0	5.2	V
I_{load}	Output current range	V_{SUP}=5.5V~30V	-	-	60	mA
ΔV_O	Voltage regulation rate	I_{load}=60mA, V_{SUP}=6V~30V	-	5	30	mV
ΔV_{OL}	Load regulation rate	V_{SUP}=24V, I_{load}=0~60mA	-	15	50	mV
I_{limit}	Short circuit protection current	-	-	10	20	mA
C_L	Load capacitance	-	2.2	4.7	100	uF
ESR	Equivalent series resistance	-	0	0	1	Ω

Table 16 Over-temperature Protection

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
OTP_{HY+}	High value of over-temperature protection	-	150	160	170	℃
OTP_{HY-}	Low value of over-temperature protection	-	125	135	145	℃
OTP_{HY}	Over-temperature protection hysteresis	-	10	25	35	℃

5 Description of Application

5.1 Recommended application circuit diagram

Figure 3 Application Circuit

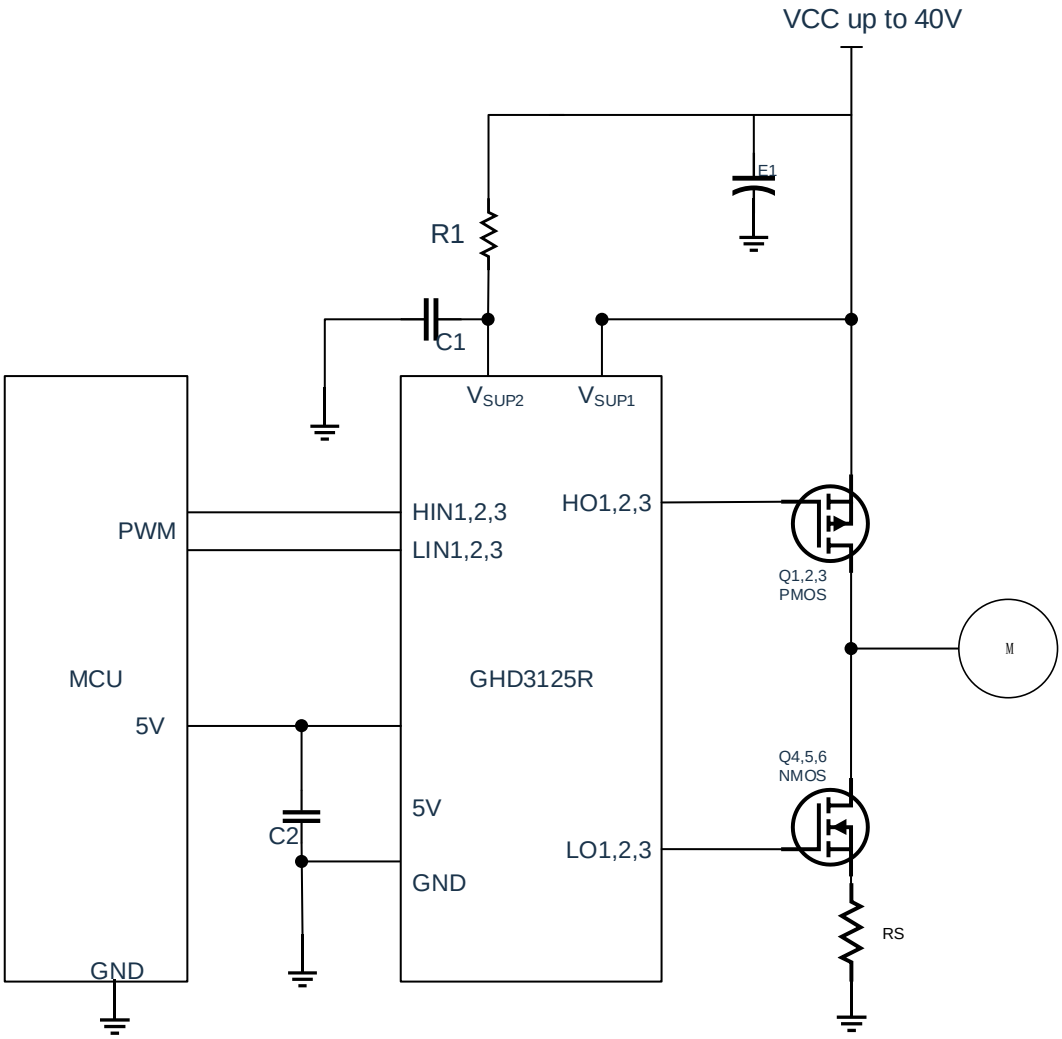


Table 17 Recommended Parameters

Position number	Name	Typical application value	Remarks
E1	Power storage capacitor	100uF/50V	Electrolytic capacitor, which requires a large capacitance value to ensure stable power supply
C1	Power filter capacitor	4.7 uF/50V	Chip capacitor, which has a capacitance value smaller than E1, and filters the power supply noise
C2	5V energy storage capacitor	2.2uF/25V	Chip capacitor, selected based on actual 5V ripple conditions
R1	V_{SUP1} voltage divider resistance	20Ω/5% (depending on the application)	Chip resistor 1206; selected based on the actual power consumption that needs to be shared

5.2 PCB layout suggestions

(1) The logic input port cannot be suspended and must be controlled by the PWM state of the microcontroller.

(2) To reduce the influence of parasitic parameters in PCB wiring, capacitors C1 and C2 should be placed as close as possible to their respective port, and the ground wire should be kept thick and short.

(3) In case of power failure, the output port impedance of the 5V circuit should be less than 150 Ω to avoid triggering internal short-circuit protection during startup.

(4) The circuit of the sampling resistor should be kept thick and short, and as close as possible to the S end of the power transistor, while the filter capacitor of the sampling signal should be close to the signal detection end.

(5) When the instantaneous overload of the 5V circuit exceeds 180mA, the short-circuit protection function will be enabled, causing the output to be turned off.

(6) The power storage capacitor E1 for V_{SUP} and GND, and the power filter capacitor C2 for 5V and GND need to form a small-area power circuit, and the circuit should be as short as possible.

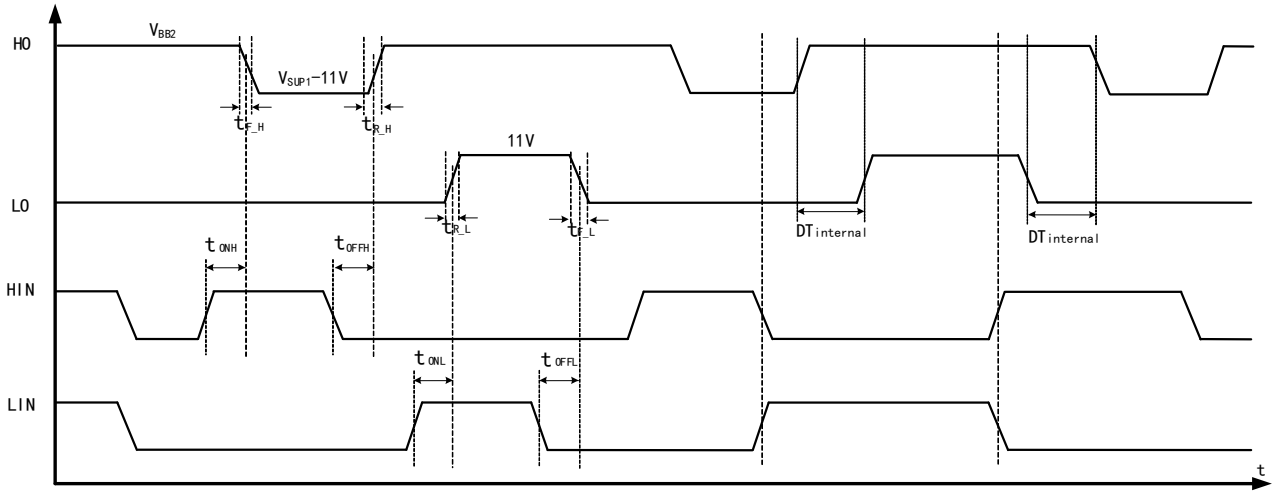
(7) The power transistor of the high-current circuit should have a small area and use thick and short circuits to reduce the voltage spike caused by parasitic inductance due to di/dt.

(8) The grounding pin and all gate-driven GND on the board should adopt star grounding to reduce mutual interference between signals.

6 Test Instructions

6.1 Time parameter definition

Figure 4 Time Parameters

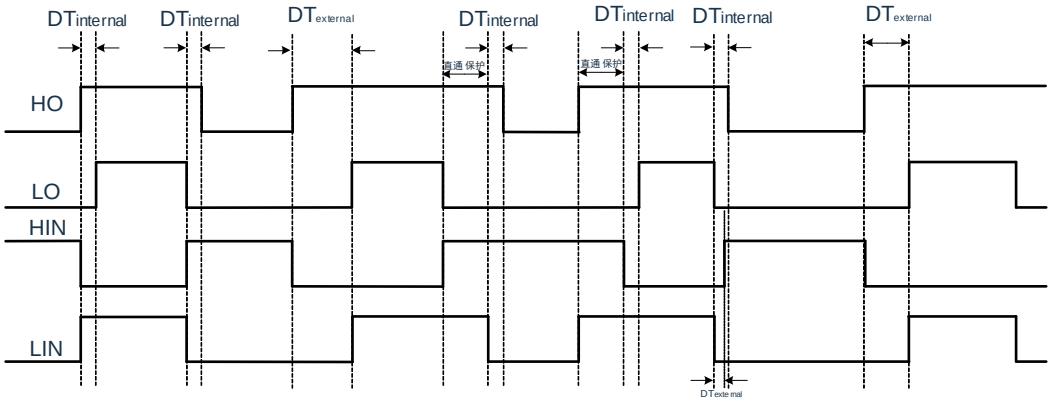


6.2 Straight-through protection and dead time test

A straight-through protection and dead time protection circuit based on the input signal is embedded in the chip. The double high level on the input logic will be determined as a straight-through signal, and the corresponding output will be set to low; moreover, it ensures that at least one dead time is embedded between the output high levels under any input condition. The logic of the external dead time DT_{ext} given on the input end and the embedded dead time DT_{int} is as follows:

- If $DT_{ext}>DT_{int}$, $DT=DT_{ext}$
- If $DT_{ext}<DT_{int}$, $DT=DT_{int}$

Figure 5 Logic Timing Diagram (ignoring transmission delay)



7 Package Information

7.1 SOP16 package information

Figure 6 SOP16 Package Diagram

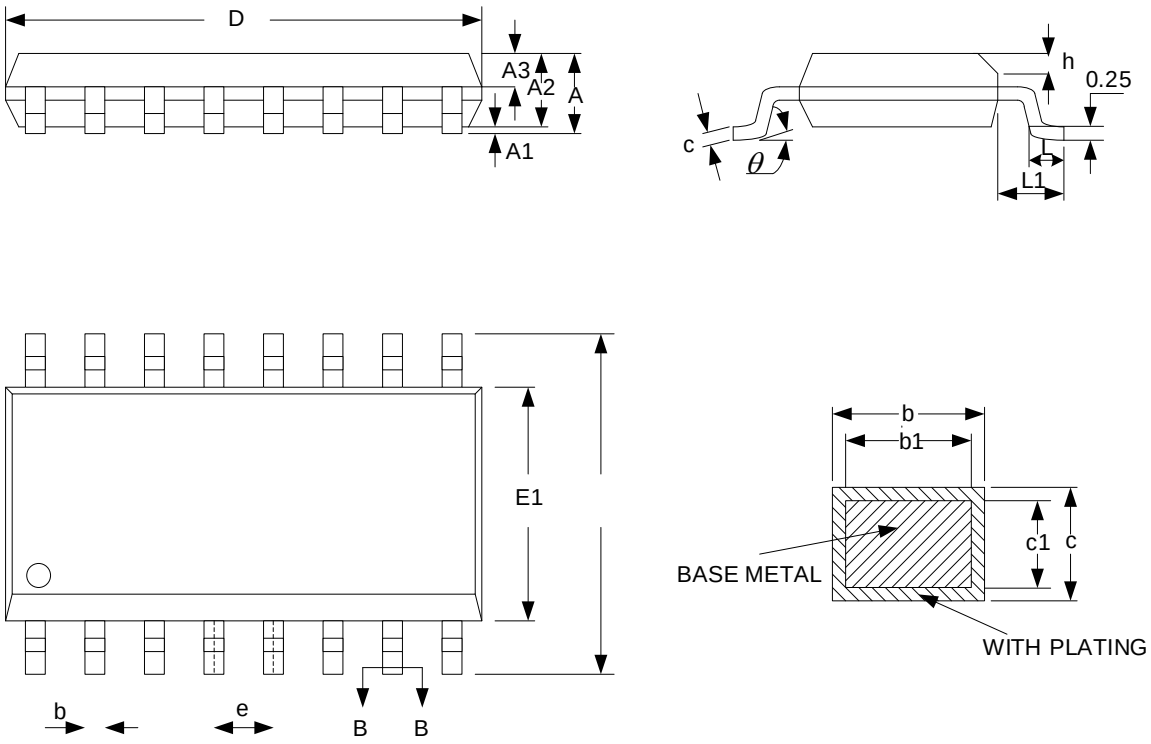


Table 18 SOP16 Package Data

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.5	-	0.80
L1	1.05REF		

SYMBOL	MILLMETER		
	MIN	NOM	MAX
θ	0°	-	8°

7.2 Package identification

Figure 7 SOP16 Package Identification

Table 19 Instructions for SOP16 Silk Screen Printing Diagram

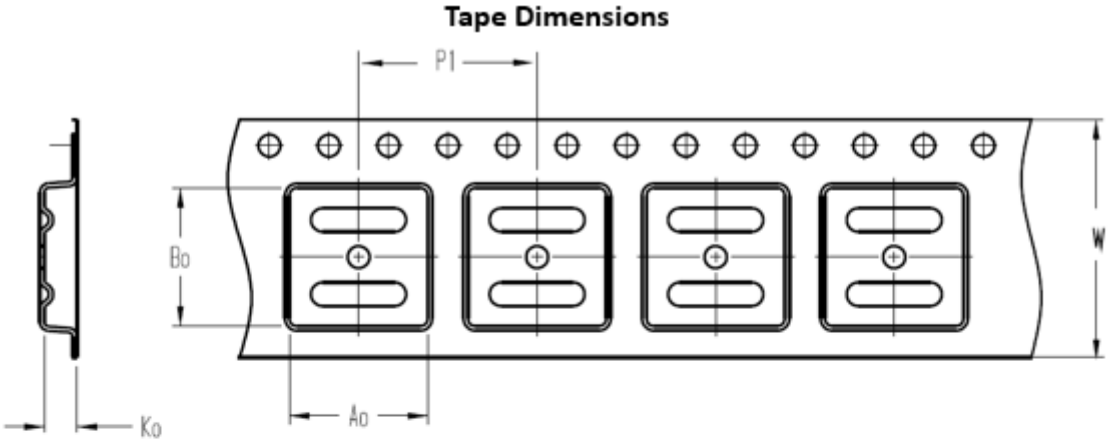
Symbol and icon	Description
XXXXXXXX	Product model
LLLLLLLLLL	Batch number
CCCC	Internal traceability code
YYWW	Year and week
●	Location of PIN1

Note: The digits for the content in each of the above column are not fixed.

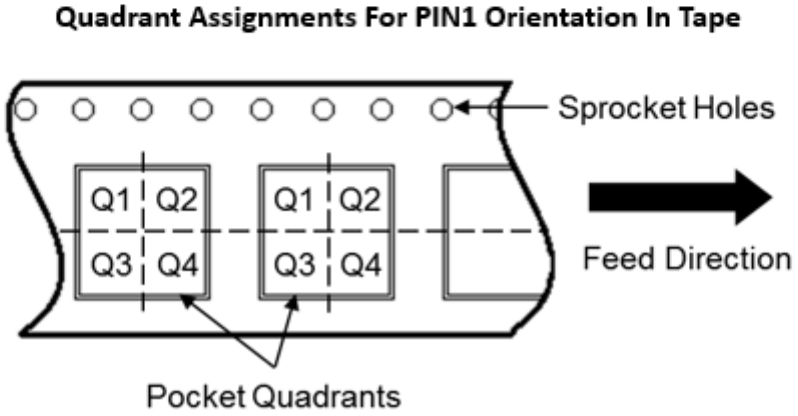
8 Packaging Information

8.1 Reel packaging

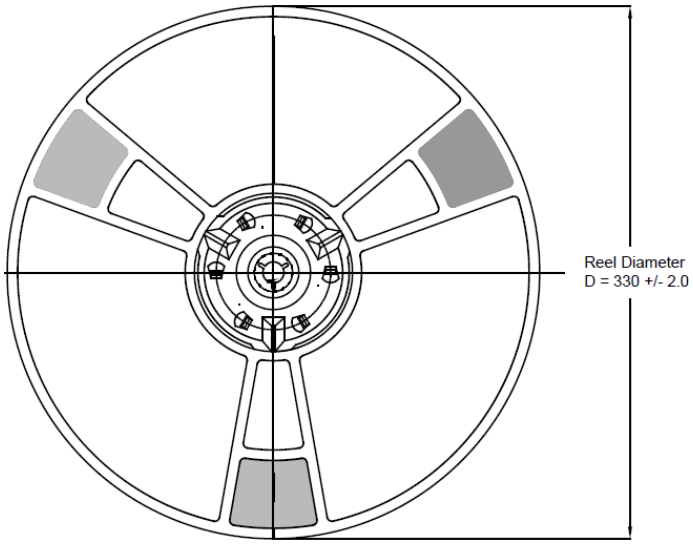
Figure 8 Reel Packaging Specification Drawing



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Reel Dimensions



Note: All photos are for reference only, and the appearance is subject to the product.

Table 20 Parameter Specification Table of Reel Packaging

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	P1 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
GHD3125R	SOP	16	3000	330	6.7	10.4	8	2.1	16	Q1

8.2 Material tube packaging

Figur 9 Material Tube Packaging Diagram

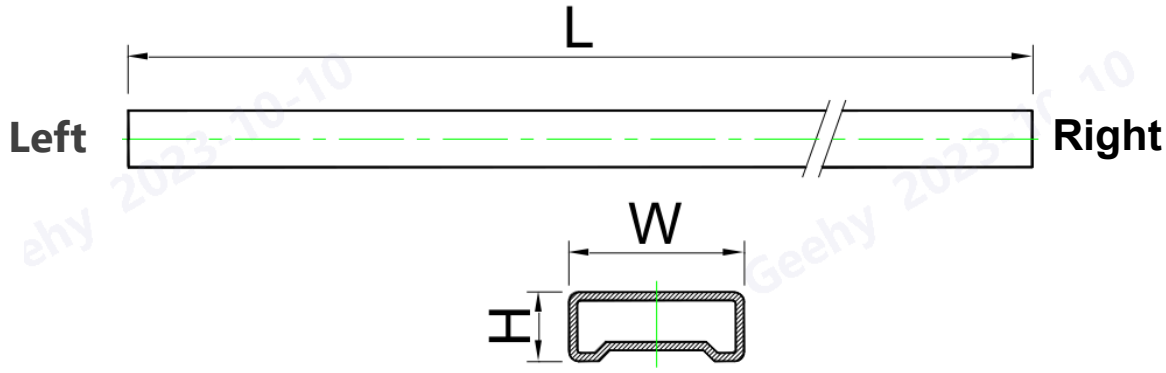


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Table 21 Parameter Specification Table of Material Tube Packaging

Device	Package Type	Pins	Qty Per Tube	SPQ	L (mm)	W (mm)	H (mm)
GHD3125R	SOP	16	50	5000	520	7.8	3.4

Note: SPQ= Smallest Packaging Quantity

9 Ordering Information

Table 22 Product Naming Definition

Product name			
GHD3125R			
Naming example	Definition	Naming	Information
GH	Brand	GH	Geehy
D	Driver	D	Driver
3	Channel	3	Channel
1	Voltage	1	0~40V
2	Current	2	180~450mA
5	Logic	5	PN
R	Built-in	R	LDO
N	Package	N	SOP
C	Pin	C	16 pins
R	Packaging	R	Reel packaging
		T	Material tube packaging

Table 23 Ordering Information List

Order code	Package	SPQ	Temperature range
GHD3125R -R	SOP16	3000	Industrial grade -40℃~85℃
GHD3125R -T	SOP16	5000	Industrial grade -40℃~85℃

10 Revision

Table 24 Document Revision History

Date	Version	Change History
2025.3	1.0	New

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